This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1-49. (Canceled)

50. (Previously presented) A semiconductor package comprising:

a first semiconductor chip having opposed first and second surfaces, the second surface including a plurality of pads;

a plurality of conductive wires, wherein each of the conductive wires is electrically coupled to a respective one of the pads of the first semiconductor chip;

a second semiconductor chip stacked over the second surface of the first semiconductor chip, the second semiconductor chip including a first surface, and an opposite second surface that includes a plurality of pads;

an insulator coupled to and covering the entire first surface of the second semiconductor chip, said insulator being vertically between each of the conductive wires and the first surface of the second semiconductor chip;

an adhesive layer attached to the insulator and the second surface of the first semiconductor chip; and

a sealing material covering the first and second semiconductor chips, wherein a portion of the sealing material is vertically between the pads of the second surface of the first semiconductor chip and the insulator.

51. (Previously presented) A semiconductor package comprising:

a first semiconductor chip having opposed first and second surfaces, the second surface including a plurality of pads;

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a plurality of conductive wires, wherein each of the conductive wires is electrically coupled to a respective one of the pads of the first semiconductor chip;

a second semiconductor chip stacked over the second surface of the first semiconductor chip, the second semiconductor chip including a first surface, and an opposite second surface that includes a plurality of pads;

an insulator coupled to and covering the entire first surface of the second semiconductor chip, said insulator being vertically between the pads of the second surface of the first semiconductor chip and the first surface of the second semiconductor chip; and

an adhesive layer attached to the insulator and the second surface of the first semiconductor chip, the adhesive layer being entirely inward of the pads of the second surface of the first semiconductor chip.

52. (Previously presented) A semiconductor package in accordance with Claim 51, further comprising a sealing material covering the first and second semiconductor chips, wherein a portion of the sealing material is vertically between the pads of the second surface of the first semiconductor chip and the insulator.

53-65. (Canceled)

66. (New) A semiconductor package in accordance with Claim 50 wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

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67. (New) A semiconductor package in accordance with Claim 50 wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

68. (New) A semiconductor package in accordance with Claim 50 further comprising a substrate, the first semiconductor chip being coupled to the substrate.

69. (New) A semiconductor package in accordance with Claim 68 wherein the substrate is selected from the group consisting of a printed circuit board, a circuit tape, and a lead frame.

70. (New) A semiconductor package in accordance with Claim 68 wherein the substrate comprises:

a resin layer;

top circuit patterns;

bottom circuit patterns; and

vias connecting the top circuit patterns and the bottom circuit patterns.

71. (New) A semiconductor package in accordance with Claim 70 further comprising conductive balls fused to the bottom circuit patterns.

72. (New) A semiconductor package in accordance with Claim 68 wherein the substrate comprises:

a chip mounting plate, the first semiconductor chip being coupled to the chip mounting plate; and

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a plurality of leads formed outside of the chip mounting plate.

73. (New) A semiconductor package in accordance with Claim 50 further comprising a substrate comprising a perforating hole, the first semiconductor chip being locate in the perforating hole.

74. (New) A semiconductor package in accordance with Claim 50 further comprising a substrate, wherein first ends of the conductive wires are bonded on the substrate by ball bonding and second ends of the conductive wires are bonded on the pads of the first semiconductor chip by stitch bonding.

75. (New) A semiconductor package in accordance with Claim 50 further comprising a substrate, wherein first ends of the conductive wires are bonded on the substrate and second ends of the conductive wires are bonded on the pads of the first semiconductor chip by stitch bonding.

76. (New) A semiconductor package in accordance with Claim 50 further comprising a substrate, wherein first ends of the conductive wires are bonded on the substrate by ball bonding and second ends of the conductive wires are bonded on the pads of the first semiconductor chip.

77. (New) A semiconductor package in accordance with Claim 50 wherein the first semiconductor chip is an edge pad type semiconductor chip in which the pads of the first semiconductor chip are formed at an inner circumference of the second surface.

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78. (New) A semiconductor package in accordance with Claim 50 wherein sections of the conductive wires are contacted with the insulator.

79. (New) A semiconductor package in accordance with Claim 50 further comprising:

a substrate, the first semiconductor chip being coupled to the substrate; and

second conductive wires connecting the pads of the second semiconductor chip and the substrate.

80. (New) A semiconductor package in accordance with Claim 51 wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

81. (New) A semiconductor package in accordance with Claim 51 wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

82. (New) A semiconductor package in accordance with Claim 51 further comprising a substrate, the first semiconductor chip being coupled to the substrate.

83. (New) A semiconductor package in accordance with Claim 82 wherein the substrate is selected from the group consisting of a printed circuit board, a circuit tape, and a lead frame.

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84. (New) A semiconductor package in accordance with Claim 82 wherein the substrate comprises:

a resin layer;

top circuit patterns;

bottom circuit patterns; and

vias connecting the top circuit patterns and the bottom circuit patterns.

85. (New) A semiconductor package in accordance with Claim 84 further comprising conductive balls fused to the bottom circuit patterns.

86. (New) A semiconductor package in accordance with Claim 82 wherein the substrate comprises:

a chip mounting plate, the first semiconductor chip being coupled to the chip mounting plate; and

a plurality of leads formed outside of the chip mounting plate.

87. (New) A semiconductor package in accordance with Claim 51 further comprising a substrate comprising a perforating hole, the first semiconductor chip being locate in the perforating hole.

88. (New) A semiconductor package in accordance with Claim 51 further comprising a substrate, wherein first ends of the conductive wires are bonded on the substrate by ball bonding and second ends of the conductive wires are bonded on the pads of the first semiconductor chip by stitch bonding.

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89. (New) A semiconductor package in accordance with Claim 51 further comprising a substrate, wherein first ends of the conductive wires are bonded on the substrate and second ends of the conductive wires are bonded on the pads of the first semiconductor chip by stitch bonding.

90. (New) A semiconductor package in accordance with Claim 51 further comprising a substrate, wherein first ends of the conductive wires are bonded on the substrate by ball bonding and second ends of the conductive wires are bonded on the pads of the first semiconductor chip.

91. (New) A semiconductor package in accordance with Claim 51 wherein the first semiconductor chip is an edge pad type semiconductor chip in which the pads of the first semiconductor chip are formed at an inner circumference of the second surface.

92. (New) A semiconductor package in accordance with Claim 51 wherein sections of the conductive wires are contacted with the insulator.

93. (New) A semiconductor package in accordance with Claim 51 further comprising:

a substrate, the first semiconductor chip being coupled to the substrate; and

second conductive wires connecting the pads of the second semiconductor chip and the substrate.

94. (New) A semiconductor package in accordance with Claim 51 wherein the conductive wires are selected from the

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group consisting of gold wires, copper wires and aluminum wires.

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